REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated August 13, 2003 (U.S. Patent Office Paper No. 2). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1 to 11 are pending in this application. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1 to 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Barnes, U.S. Patent No. 6,122,315 (further, the '315 patent). Applicants respectfully traverse the rejection.

Claim 1 recites a digital data decompressing system that decompresses compressed digital data to restore original data thereof, comprising plural memory areas in which the decompressed data is stored, and flags, provided so as to correspond one for one with the plural memory areas, which indicate whether stored data is all predetermined logical values, wherein, when data to be written to the memory areas is all predetermined logical values, the corresponding flags are set to a first state.

The Examiner alleges in the Office Action, page 2, that the '315 patent discloses in the abstract, in Fig. 6, in Fig. 9c, in col. 10, lines 30+ and in col. 11, lines 1+ the recitation of claim 1. However, the Examiner also points out that the '315 patent fails to explicitly teach a predetermined logical value, but teaches the logical values and plurality of memory areas and status flag and four states of logical values "which makes it obvious that the four state of logical values are preset or predetermined logical values." Applicants respectfully disagree.

The '315 patent in fact discloses a memory controller for a MPEG decoder. This memory controller controls memory states by a four state output 110, as explained in the '315 patent in col. 10, lines 36 to 39. The four state output 110 is produced from signals of block 100 and block 102 which are state machines for the writeback process and the raster process. The '315 patent discloses in col. 10, lines 26 to 28 that "Block 100 and the block 102 are state machines for the writeback process and the raster process discussed above,

respectively." A writeback process 66 and a raster process 82 are described in col. 7, lines 55 to 63 and col. 8, lines 11 to 29. As described in the above referenced paragraphs, the writeback process and the raster process do not work according to predetermined logical values which are determined from data in memory areas, as recited in claim 1. The four state output 110 is merely a signal for controlling the memory controller. Therefore, Applicants respectfully submit that the four state output 110 is different than the flags recited by claim 1.

In contrast, the flag recited by claim 1 is a flag for indicating predetermined logical values of data stored in memory areas. By referring to an all-zero flag, the control circuit can avoid a wasted writing/reading process whereby implicitly power consumption is lowered and computation time is shortened. The '315 patent does not disclose, teach or suggest the controlling of the flags according to predetermined logical values of data stored in memory areas. Therefore, the invention recited by claim 1 is not obvious in view of the '315 patent. Based on the above, Applicants respectfully ask the Examiner to widthraw the rejection of claim 1.

Claims 2 to 8 depend from and add features to allowable claim 1. Therefore, they are allowable at least for the reasons discussed above regarding claim 1.

Regarding claims 9 to 11, the Examiner alleges on page 3 of the office action that "the claimed limitations are substantially similar to claims 1 to 4, therefore the grounds for rejecting claims 1 to 4 also apply here." Applicants respectfully disagree that claims 9 to 11 are obvious in light of the '315 patent.

Claims 9 to 11 recite the steps of a method that takes place in "a digital data decompressing system that comprises plural memory areas in which decompressed data is stored, flags, provided so as to correspond one for one with the plural memory areas, which indicate whether stored data is all logical "0"s, and an arithmetic circuit for performing computations between data items stored in the memory areas." As discussed above in connection with claims 1 to 8, the decompressing system comprises a flag, that in case of claims 9 to 11 is an all-zero flag. By referring to the all-zero flag, the control circuit can avoid wasted writing/reading, decrease its power consumption and shorten the computation time. The '315 patent does not disclose, teach or suggest the controlling of flags according to predetermined logical values of data stored in memory areas. Therefore, the method recited by claims 9 to 11 is not obvious in light of the disclosure of the '315 patent. Based on the above, Applicants respectfully ask the Examiner to withdraw the rejection regarding claims 9 to 11.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

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November 6, 2003